AN10767

Enhanced BOD function of the LPC9351

Rev. 01 — 2 December 2008 Application note

Document information

Info	Content
Keywords	LPC9351, enhanced BOD, brownout detect
Abstract	This application note describes how to use enhanced BOD function in LPC9351. Demo code is also provided.

Revision history

Rev	Date	Description
01	20081202	Initial version.

Contact information

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1. Introduction

The brownout detect function determines if the power supply voltage drops below a certain level. The Enhanced BOD feature of the P89LPC9351 has 3 independent functions: BOD reset, BOD interrupt and BOD EEPROM/FLASH.

2. BOD EEPROM/FLASH

BOD EEPROM/FLASH is used for flash/Data EEPROM program/erase protection. BOD EEPROM/FLASH is always on, except in power-down or total power down mode (PCON.1=1). It can not be disabled in software. BOD EEPROM/FLASH has only 1 trip voltage level of 2.4V.

For 512 bytes on-chip DATA EEPROM, EWERR1 and EWERR0 bit in the DEECON register are used to indicate a write error of the BOD EEPROM. The EWERR0 bit is '1' when V_{DD} falls below 2.4V during program/erase operation. The EWERR1 bit will be '1' when a program/erase is requested and V_{DD} lower than 2.4V. Both bits can be cleared by power on reset, watchdog reset or a software write. Please refer to P89LPC9351 User manual on how to use these two bits.

For the 8K bytes of on-chip flash, the BOD FLASH is tripped and flash erase/program is blocked when V_{DD} is lower than 2.4V. The HVA bit in the FMCON register indicates the BOD FLASH occurred.

3. BOD Reset and BOD Interrupt

A BOD reset will cause a processor reset and it is always on, except in total power-down mode. It could not be disabled in software. The BOD interrupt will generate an interrupt and can be enabled or disabled in software.

The BOD reset and BOD interrupt each has 4 trip voltage levels. BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are used as trip point configuration bits of BOD reset. BOICFG1 bit and BOICFG0 bit in the BODCFG register are used as trip point configuration bits for the BOD interrupt. The BOD reset voltage should be lower than the BOD interrupt trip point. Table 2 gives BOD trip point configuration.

After power-on reset, the BOICFG1/0 bits will be copied from UCFG1.5 and UCFG1.3. The factory preprogrammed value of UCFG1 is 0x63. In this case, the trip voltage level is 2.4V for BOD reset and 2.6V for BOD interrupt. Of course, you can change the trip point of the BOD interrupt in software. When configuring the trip voltage of the BOD reset, make sure the operational supply voltage is high enough. Otherwise it will cause the processor to be reset continuously.

Table 1. Flash user configuration byte 1 (UCFG1) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WDTE	RPE	BOE1	WDSE	BOE0	FOSC2	FOSC1	FOSC0
Unprogrammed value	0	1	1	0	0	0	1	1

In total power-down mode (PMOD1/PMOD0 = '11'), the circuitry for the Brownout Detection is disabled for lowest power consumption. When the PMOD1/PMOD0 bits are not equal to '11', BOD reset is always on and the BOD interrupt is enabled by setting BOI

(PCON.4) bit. Please refer to Table 3 for BOD reset and BOD interrupt configuration. BOF bit (RSTSRC.5), the BOD reset flag has a default value of '0' and is set when a BOD reset is tripped. The BOIF bit (RSTSRC.6), BOD interrupt flag is default as '0' and is set when the BOD interrupt is tripped.

Table 2. BOD trip points configuration

BOE1 (UCFG1.5)	BOE0 (UCFG1.3)	BOICFG1 (BOICFG.1)	BOICFG0 (BOICFG.0)	BOD reset	BOD interrupt
0	0	0	0	Reserved	
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1	2.2 V	2.4 V
0	1	1	0	2.2 V	2.6 V
0	1	1	1	2.2 V	3.2 V
1	0	0	0	Reserved	
1	0	0	1		
1	0	1	0	2.4 V	2.6 V
1	0	1	1	2.4 V	3.2 V
1	1	0	0	Reserved	
1	1	0	1		
1	1	1	0		
1	1	1	1	3.0 V	3.2 V

Table 3. BOD reset and BOD interrupt configuration

PMOD1/PMOD0(PCON[1:0])	BOI (PCON.4)	EBO (IEN0.5)	EA (IEN0.7)	BOD reset	BOD interrupt
11 (total power-down)	X	X	X	N	N
≠ 11 (any mode other than total power down)	0	X	X	Y	N
	1	0	X	Y	N
		X	0	Y	N
		1	1	Y	Y

4. BOD Demo

4.1 Demo introduction

This demo gives an example on how to use the enhanced BOD feature. The Keil MCB900 board is used for this application note.

In the demo, the trip voltage is set to 2.4V for a BOD reset and 3.2V for a BOD interrupt. While the LPC9351 is running, the power supply is adjusted to lower than 3.2V to trigger BOD interrupt. The ISR of the BOD interrupt will blink the eight LEDs and output “BOD interrupt” information through UART0.

The BOE1/0 bits (UCFG1.5/1.3) are set to ‘10’. The subroutine BOD_Int_Config() implements BOD interrupt initialization.

```
1    BODCFG=0xFF;          /*Set BODCFG.1,0= 1,1 ,so the BOD int voltage is 3.2V*/
2    EA=1;                 /*Set EA  */
3    EBO=1;                /*Set BOD enable  */
4    PCON |=0x10;          /*Set BOD interrupt enable  */
```

BOD interrupt ISR is implemented as below:

```
5    void BOD_ISR(void) interrupt 5
6    {
7    RSTSRC &= 0xbf;               /*clr BOIF at RSTSRC.6*/
8    printf ("\n");                /*print BOD interrupt information*/
9    printf ("BOD interrupt! Please note the voltage! \n");
10   printf ("\n");
11   P2^=0xff;                     /* Blinky LEDs */
12   delay();
13   }
```

4.2 Demo setup

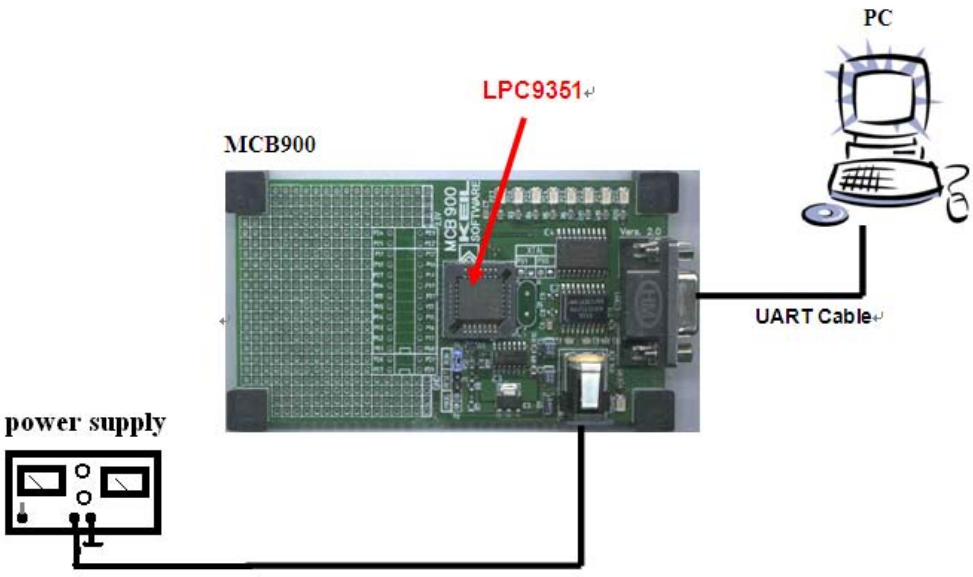

Fig 1. Demo setup

4.3 Output information

When the power supply falls to lower than about 3.2V, the BOD interrupt is triggered and debug information “BOD interrupt” will be sent to UART0. If the power supply is raised higher than 3.2V, there will be no serial debug information.

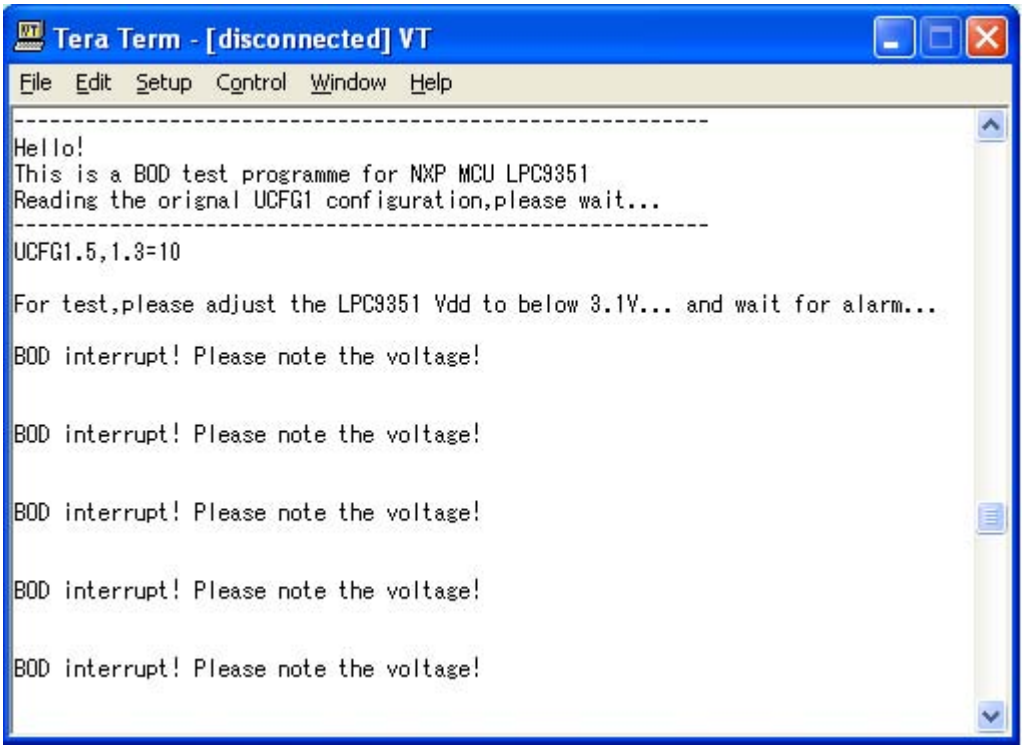

Fig 2. output information

5. Reference

[1] LPC9351 User Manual (UM10308) – Rev. 01

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Date of release: 2 December 2008
Document identifier: AN10767_1